To assure maximum dynamic range, the four biquad-filter sections (two in each IC) exhibit increasing Q from input to output. The pole-zero pairs of each section also exhibit increasing frequency, which minimizes the spread in component values. The following pole and zero values produce a 1-rad/sec filter passband:

Section	fPole (Hz)	QPole	fZero (Hz)
1	0.1005	0.5603	0.2397
2	0.1310	1.0540	0.2777
3	0.1564	2.3876	0.4273
4	0.1685	8.5145	1.4016

Note the feedback capacitors C1-C4 across each output op amp. These capacitors have two purposes: they improve the quality of transmission zeroes, and they form 1-pole lowpass filters that help to smooth out the discrete-level steps introduced by the filter's switched-capacitor action. The 1-pole filters have little effect on the passband shape because their high corner frequencies introduce only 0.1dB of loss at 1kHz.

Note also, that the applied clock frequency in Figure 2 (192kHz) allows use of a convenient binary-64 divider for setting the necessary 3X ratio between the converter's sample rate and the filter's 1-kHz corner frequency, f_0. Each chip is programmed for an f_{CLK}/f_0 ratio of 191.64 by V^+ and V^- connections to the filter inputs, F0-F5.

(Circle 2)

D/A-converter generates multiple precision outputs

The Figure 1 circuit creates four channels of buffered, precision-voltage output channels from a single high-resolution D/A converter. The relatively low parts count depends on a low-leakage, four-channel differential multiplexer (IC5), which directs the converter's output to each of four low-leakage 0.1µF hold capacitors. Output buffers reside in a CMOS quad op amp (IC6).

To reduce signal offset contributed by the multiplexer and output buffers, the circuit includes these components in the feedback path of op amp IC4. This arrangement lowers any such offset by a factor of 97 (the closed-loop gain of IC4), although IC4's offset (15µV max at 25°C) remains in effect.

Specialized multiplexer IC5 provides the low current leakage and low charge injection required by the four sample/hold circuits. Its 4pC typical charge injection, for instance, produces a 40µV offset at each hold capacitor. Summing this error with the IC4 offset (10µV typical) and the offset of a buffer amplifier (5mV divided by 97, or 52µV typical) gives a total of 102µV, which is approximately 2/3 of an LSB (2.5V divided by 2^{14}, or 152µV).

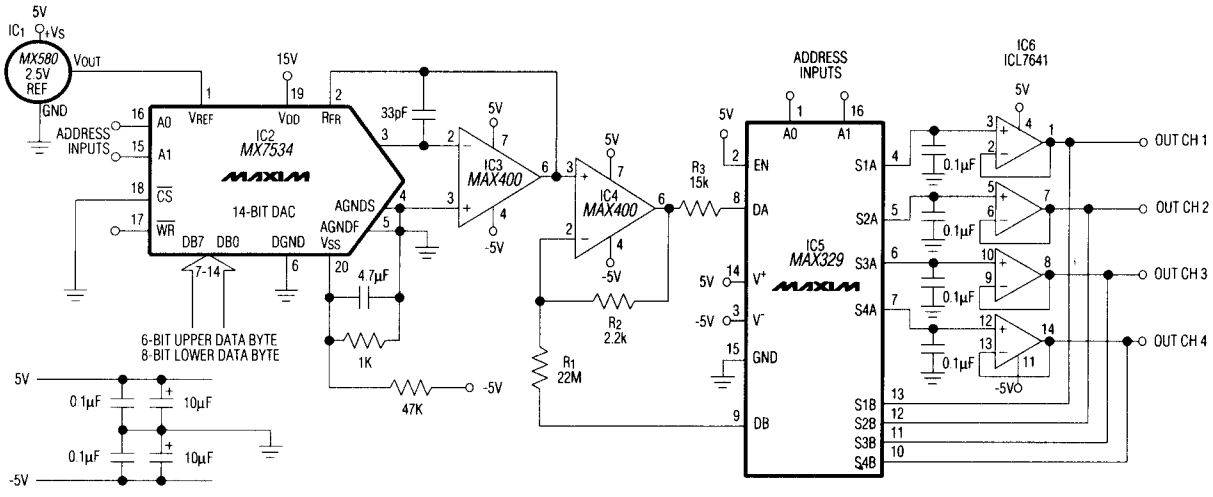

Figure 1. An output multiplexer and four buffers enable a high-resolution D/A converter to generate four channels of precision output voltage.

Each hold capacitor can therefore discharge about 50µV before the net error equals one LSB. Typical room-temperature leakages in the mux (1pA) and buffer (1pA) will discharge a hold capacitor by 50µV in about 2.5 seconds. Maximum room-temp leakages, on the other hand (25pA in the mux and 50pA in the buffer), will discharge the capacitor by 50µV in only 67msec. At higher temperature, the discharge is even faster.

You can compensate a given rate of hold-capacitor discharge by simply clocking the multiplexer fast enough to recharge the capacitors, while simultaneously updating the converter output as required for each channel. During power-up or when changing a channel voltage, however, the system may require several multiplexer cycles to establish the capacitor voltage.

Eliminating R3 (at the output of IC4) would reduce the capacitor-charge time. Similarly, eliminating the gain network R2/R1 around IC4 would further reduce output offset by applying the op amp's full open-loop gain to the mux-buffer loop. These three resistors, however, assure the loop's stability.

R_3 and the multiplexer on-resistance form a pole with each hold capacitor that reduces the 40dB low-frequency gain of op amp IC4 to 0dB at approximately 10kHz. According to the plot of typical gain vs frequency for the op amp, the 40dB closed-loop gain also begins to fall at 10kHz, assuring loop stability by producing a 45° phase margin at that point. On the other hand, if you increase this closed-loop gain (the R2/R1 ratio), stability requires that you also increase R3, which further increases the capacitors' charge time.

(Circle 3)

Low-power op amp reduces cable costs

The extremely high source impedance of a pH probe ($10^{12}\Omega$) often mandates the use of low-loss Teflon cable between the probe and its meter electronics. Such cable costs several dollars per foot. As an alternative, you can buffer the probe with a MAX406 low-power op amp that allows the use of ordinary, less-expensive coaxial cable instead. The resulting system (Figure 1) includes a general-purpose pH electrode, a buffer circuit, and a simple LCD-meter circuit based on a $3^1/2$-digit, integrating-type A/D converter (IC2).

If desired, you can install the op amp and its power supply (a small lithium battery) within the probe housing. The entire probe-interface circuit consumes less than 1.5µA, and operates for thousands of hours on the DL1620B lithium cell shown.

The resistive divider R1/R2, whose output is midway between the 3V battery's terminals, provides a reference potential for the pH probe. This potential, connected via the coax shield to pin 32 of IC2, also establishes a common-mode reference for the A/D converter. (Pin 32 is generally 3V below the converter's V^+ level at pin 1.) Potentiometer R_3 introduces an adjustable 700mV offset. By shifting the probe's ±700mV output range to one of 0 to 1400mV, this offset provides an output compatible with the intended display range of 0 to 14 pH.

(Circle 4)

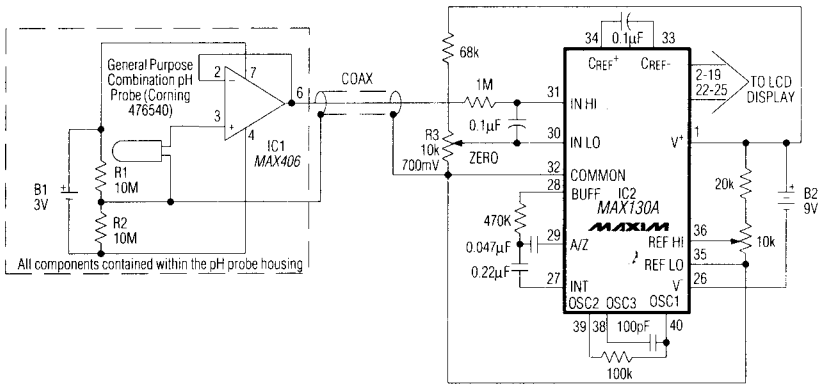

Figure 1. Adding a low-power op amp buffer (IC_1) to the output of a high-impedance pH probe allows use of ordinary coaxial cable in place of the expensive Teflon cable otherwise required.